NORIDEL HERRON

Computer Engineering | Software | Embedded Systems | FPGA/RTL
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PROFESSIONAL SUMMARY

Computer Engineering graduate with hands-on experience in programming, embedded systems, FPGA/RTL development, and hardware/software integration through academic and personal projects. Experience working with Python, C/C++, VHDL, Verilog, and SystemVerilog, with a strong foundation in computer architecture, digital design, verification, and system-level debugging. Seeking an entry-level software or computer engineering position where I can apply technical and problem-solving skills while continuing to grow as an engineer.

EDUCATION

University of Missouri - Columbia
B.S. Computer Engineering | May 2026 | GPA: 3.29

Moberly Area Community College
A.S. Engineering | Dec 2023 | GPA: 3.78

TECHNICAL SKILLS

Programming: Python, C/C++
HDL / RTL: VHDL, Verilog, SystemVerilog; RTL design; testbench development; functional verification
Computer Architecture: 5-stage pipelines, superscalar architecture, hazard detection, forwarding, stalls, branch handling
FPGA: AMD Vivado, AMD Kria KV260, Artix-7
Embedded Systems: Raspberry Pi, ESP32, hardware/software integration
Tools: Linux, GitHub, Visual Studio / VS Code, MATLAB, simulation and waveform debugging

SELECTED ENGINEERING PROJECTS

Convolutional Neural Network (CNN) FPGA Accelerator **Jan-May 2026**
| *Research Project*
- Designed and verified a VHDL-based CNN implementation on an AMD Kria KV260 FPGA.
- Created Python golden-reference models and automated testbenches for functional validation, debugging, and performance evaluation.

Uninterruptible Power Supply (UPS) / Power Control **Aug 2025-May 2026**
Unit | *Capstone Project*
- Collaborated with a multidisciplinary engineering team to develop an integrated power-control system and led software development efforts.
- Contributed to system architecture, hardware/software integration, testing, debugging, and technical problem solving.

Power Monitoring System | *Embedded Systems Class* **Sep-Dec 2025**
Project
- Designed a Raspberry Pi and ESP32-based distributed power-monitoring system.
- Developed Python tools to generate and transmit test energy data for communication testing, analysis, troubleshooting, and system verification.

Superscalar RISC-V Processor | *Personal Project* **Mar-May 2025**
- Designed and verified a 5-stage superscalar RISC-V processor in VHDL with stalling and hazard-management logic.
- Developed a custom RISC-V code generator to create hazard-inducing instruction sequences for functional verification and debugging.

Pipelined RISC-V CPU | *Personal Project* **Jan-Aug 2025**
- Designed and verified a 5-stage pipelined RISC-V processor in VHDL/Verilog with branch handling, stalling, forwarding, and hazard detection.
- Validated processor behavior through simulation, testbench development, and waveform-based debugging.

Digital Image Processing | *Class Project* **Oct-Dec 2025**
- Implemented and evaluated image enhancement, segmentation, histogram processing, contrast adjustment, and morphological algorithms using Python.